Key Parameters

V_{DSM} = 2800 V
I_{TAVM} = 2350 A
I_{TRMS} = 3680 A
I_{TSM} = 43000 A
V_{TO} = 0.85 V
r_T = 0.160 mΩ

Phase Control Thyristor

5STP 24L2800

Doc. No. 5SYA 1029-02 Dec.95

Features

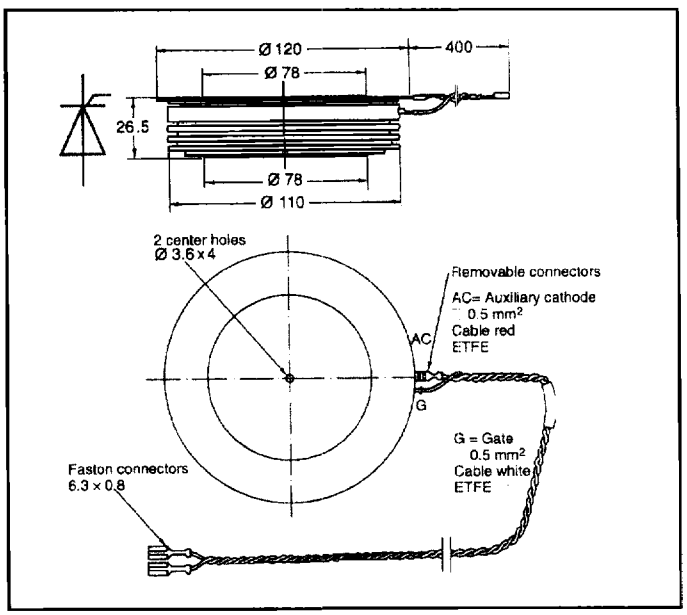
- **Patented free-floating silicon technology**
- **Designed for traction, energy and industrial applications**
- **Optimum power handling capability**

Blocking

Part number	5STP 24L2800	5STP 24L2600	5STP 24L2200	Conditions	
V_{DRM} V_{RRM}	2800 V	2600 V	2200 V	f = 50Hz, t_p = 10ms	
V_{RSM1}	3000 V	2800 V	2400 V	t_p= 5ms, single pulse	
I_{DRM}	≤ 300 mA			V_{DRM}	T_{vj} = 125°C
I_{RRM}	≤ 300 mA			V_{RRM}	
dv/dt_{crit}	1000 V/µs		@ Exp.to 0.67xV_{DR}		

Mechanical data

F_m	Mounting force	nom	50 kN
		min	45 kN
		max	60 kN
a	Acceleration Device clamped		100 m/s²
m	Weight		1.35 kg
D_s	Surface creepage distance		35 mm
D_a	Air strike distance		14 mm



On-state

I_{TAVM}	Max. average on-state current	2350 A	Half sine wave, T_c = 70°C	
I_{TRMS}	Max. RMS on-state current	3680 A		
I_{TSM}	Max. peak non-repetitive surge current	43000 A	t_p = 10 ms	T_{vj} = 125°C
		46000 A	t_p = 8.3 ms	
I^2t	Limiting load integral	9245 kA²s	t_p = 10 ms	
		8781 kA²s	t_p = 8.3 ms	
V_T	On-state voltage	1.35 V	I_T = 3000 A	
V_{TO}	Threshold voltage	0.85 V		
r_T	Slope resistance	0.160 mΩ	I_T = 1500 - 4500 A	
I_H	Holding current	20-70 mA	T_{vj} = 25°C	
		15-60 mA	T_{vj} = 125°C	
I_L	Latching current	80-300 mA	T_{vj} = 25°C	
		70-250 mA	T_{vj} = 125°C	

Switching

di/dt_{crit}	Critical rate of rise of on-state current	150 A/µs	Cont.	$V_D \leq 0.67 \times V_{DRM}$ T_{vj} = 125°C	
		300 A/µs	60 sec.	I_{TRM} = 3000 A f = 50Hz	
				I_{FG} = 2.0 A t_r = 0.5µs	
t_d	Delay time	≤ 3.0 µs	V_D =0.4xV_{DRM}	I_{FG} = 2.0 A t_r = 0.5µs	
t_q	Turn-off time	≤ 400 µs	V_D ≤0.67xV_{DRM}	I_{TRM} = 3000 A T_{vj} = 125°C	
			dv_D/dt=20 V/µs	V_R > 200 V	
Q	Recovery charge min	4000 µAs		di_T/dt= -20 A/µs	
	max	7000 µAs			

Triggering

V_{GT}	Gate trigger voltage	2.6 V	T_{vj} = 25°C
I_{GT}	Gate trigger current	400 mA	T_{vj} = 25°C
V_{GD}	Gate non-trigger voltage	0.3 V	V_D = 0.4xV_{DRM}
I_{GD}	Gate non-trigger DC current	10 mA	V_D = 0.4xV_{DRM}
V_{FGM}	Peak forward gate voltage	12 V	
I_{FGM}	Peak forward gate current	10 A	
V_{RGM}	Peak reverse gate voltage	10 V	
P_G	Gate power losses	3 W	

Thermal

$T_{vj\ max}$	Max. junction temperature	125 °C	
$T_{vj\ stg}$	Storage temperature range	-40.. ..150°C	
R_{thJC}	Thermal resistance junction to case	24 K/kW	Anode side cooled
		24 K/kW	Cathode side cooled
		12 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	10 K/kW	Single side cooled
		5 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC} = \sum_{i=1}^{n} R_i(1-e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/W)	0.0053	0.0051	0.0016	
τ_i (s)	2.1838	0.4151	0.0324	

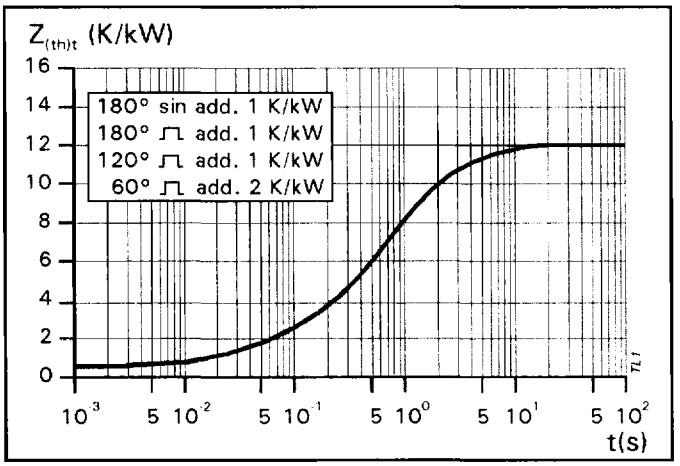


Fig.1 Transient thermal impedance, junction to case.

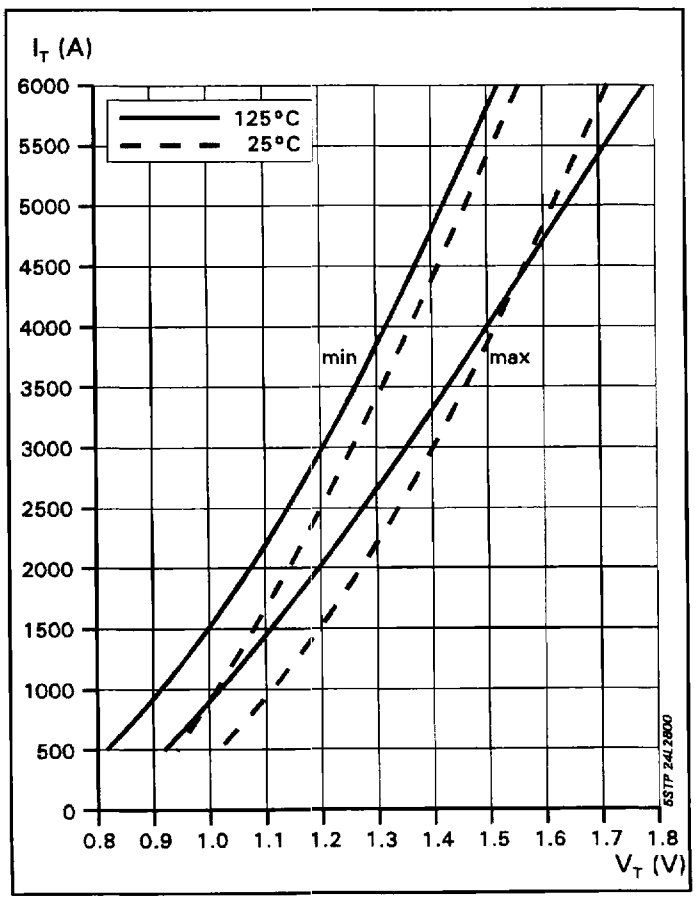


Fig.2 On-state characteristics.

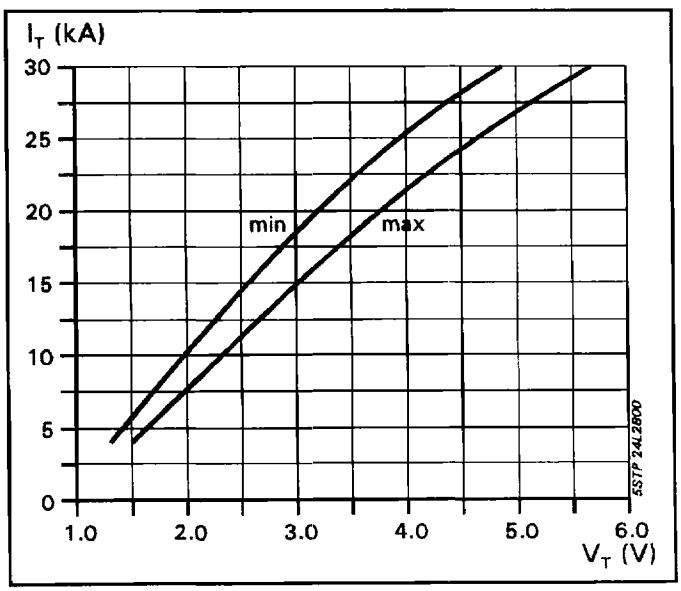


Fig.3 On-state characteristics.

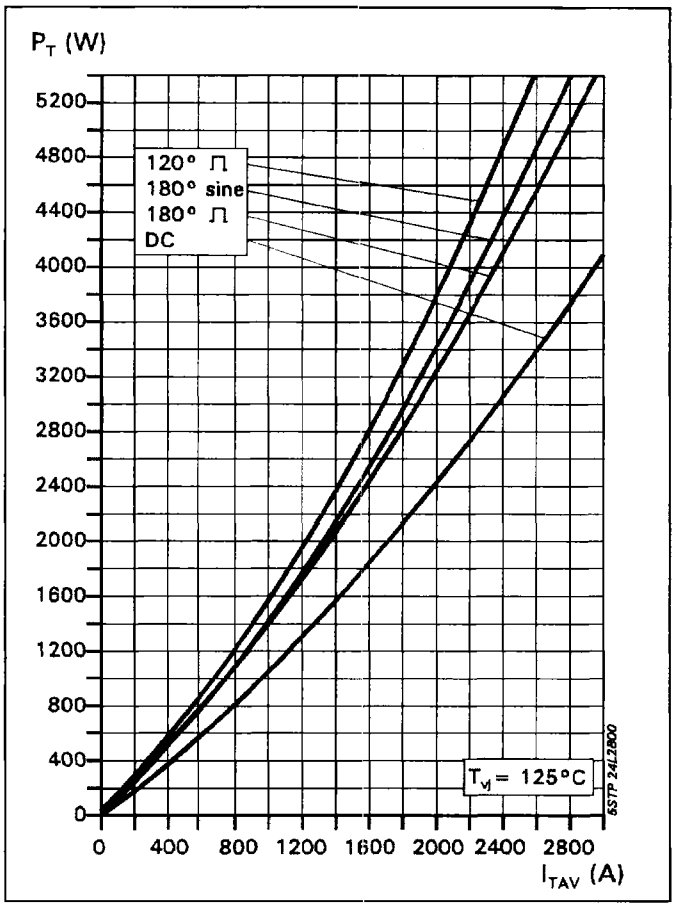


Fig.4 On-state power loss vs mean on-state current. Turn-on losses excluded.

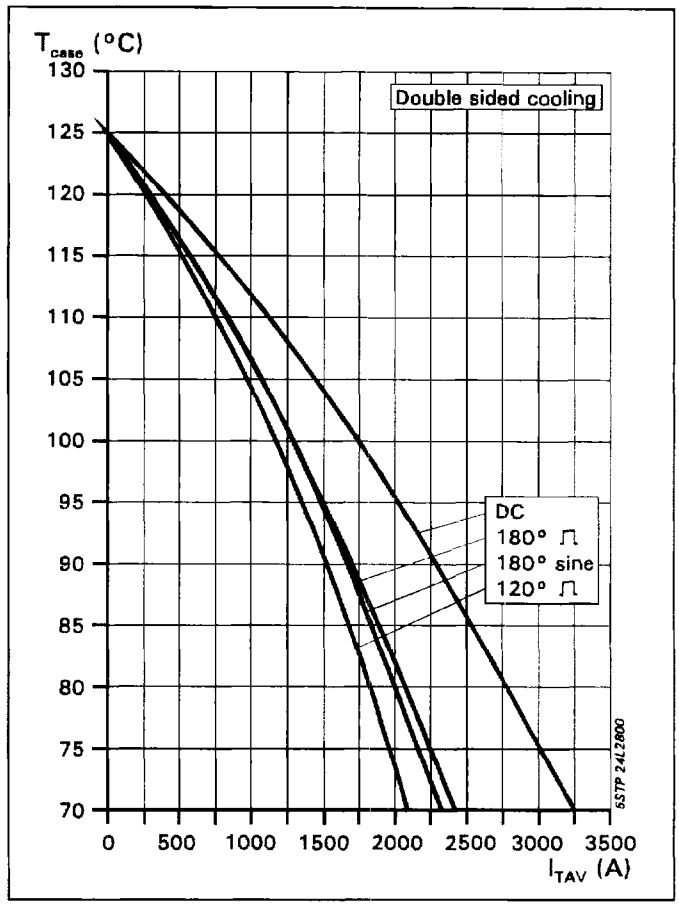


Fig.5 Max. permissible case temperature vs mean on-state current.

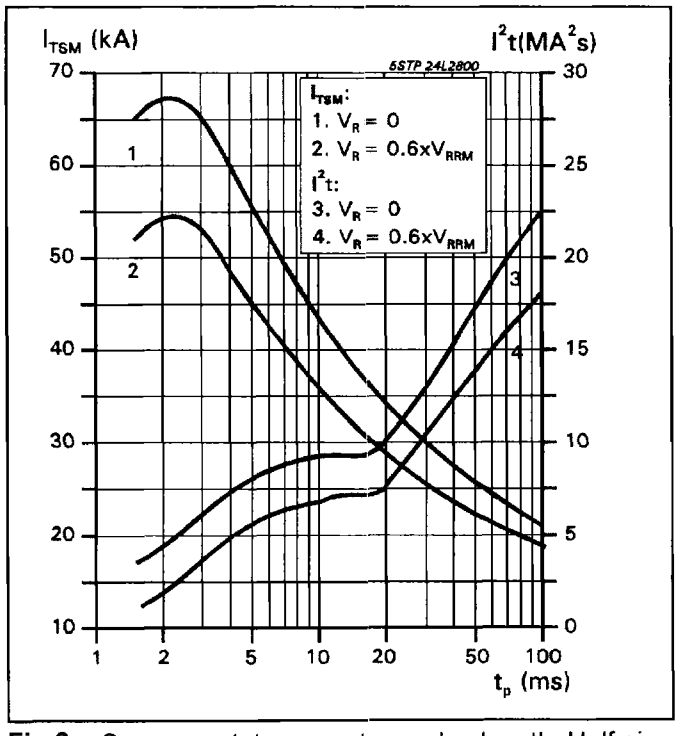


Fig.6 Surge on-state current vs pulse length. Half-sine wave.

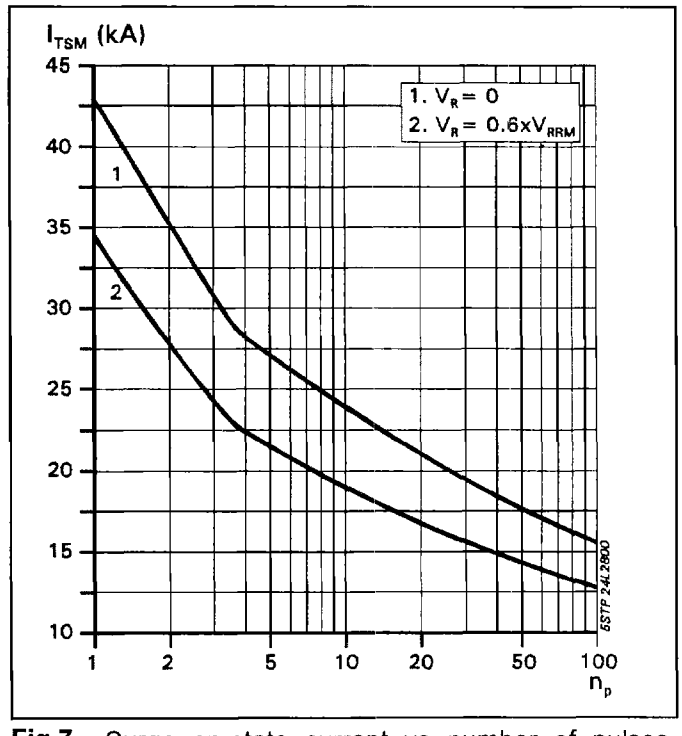


Fig.7 Surge on-state current vs number of pulses. Half-sine wave, 10ms, 50Hz.

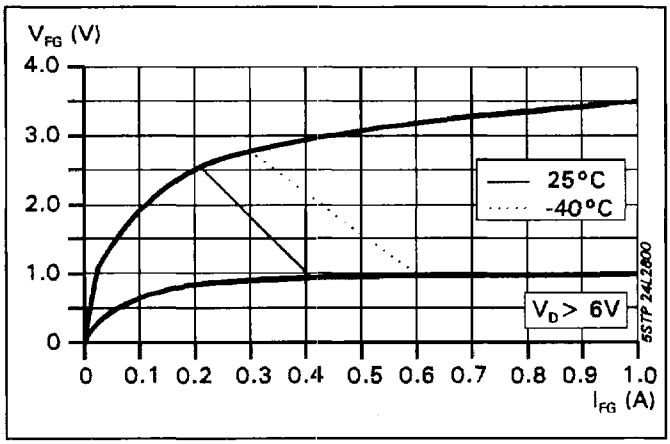


Fig.8 Gate trigger characteristics.

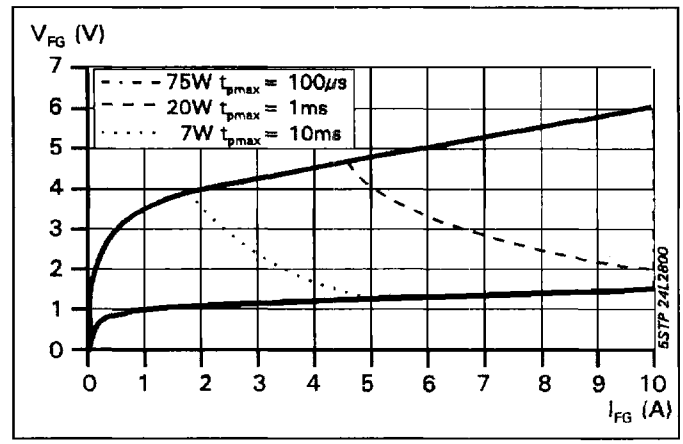


Fig.9 Max. peak gate power loss.

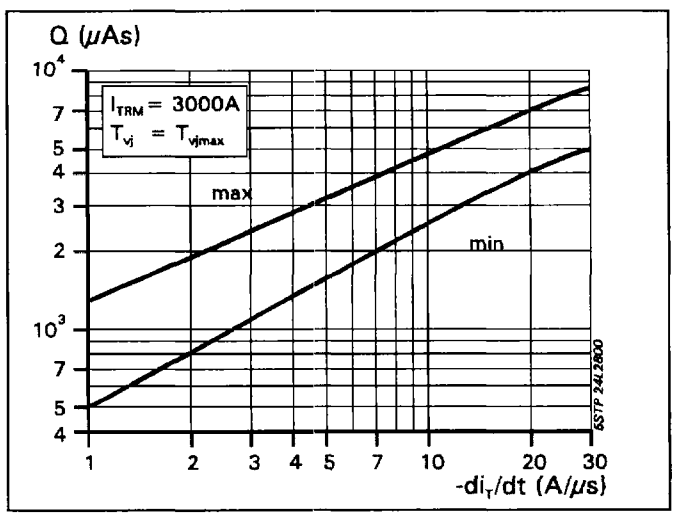


Fig.10 Recovery charge vs decay rate of on-stat current.

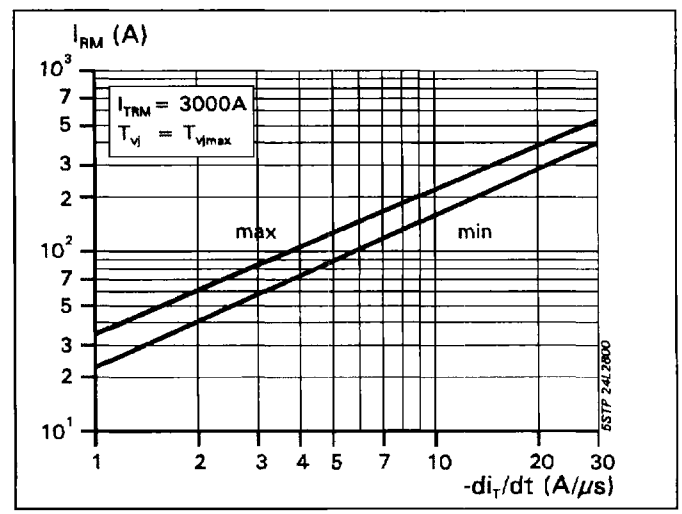


Fig.11 Peak reverse recovery current vs decay rate of on-state current.